

Plan 9 is offering a Power Line Communications (PLC) Narrow Band (9-500kHz) Transmitter Intellectual Property (IP) line driver block designed to drive the low impedance loads with outstanding linearity and MTPR (Multi-Tone Power Ratio) performance driving OFDM signals.

Applications include:

- *All PLC related standards*
- *Smart power meter communications*
- *Smart House controls*

Features of this IP Transmitter:

- *3 Amp output @ VDD-2V*
- *>500KHz Full Power Bandwidth*
- *Fully Differential Input and Single ended Output*
- *Switchable hi-impedance output mode*
- *Fixed Gain of 8V/V*
- *<50mA idle current*
- *VDD range is 10V to 24V*
- *Programmable Short circuit Protection*
- *HiZ output holding circuit*
- *IP line driver total area is less than 1.25mm²*

Description

The AC power line was not designed for data transmission. High voltage, current spikes, induced noise, switching noise, low impedance loads, lossy transmission, etc., all challenge a communication channel and the frontline AFE components but especially the line driver. The Plan 9 line-driver is designed with some of these challenges in mind.

The line driver can drive low resistive loads at high current and still maintain the low distortion needed for OFDM signals.

The short circuit current limit is designed to clip the fast-moving signal (up to 500KHz). This allows for the signal timing and crossings to be preserved during a clip. There are four choices of short circuit current.

During the output HiZ mode, the midpoint can sometimes drift from the active midpoint causing some transients during re-activation of the line driver. A mid-point hold circuit is used to keep the voltage during HiZ mode but not lower the open impedance at working frequencies.

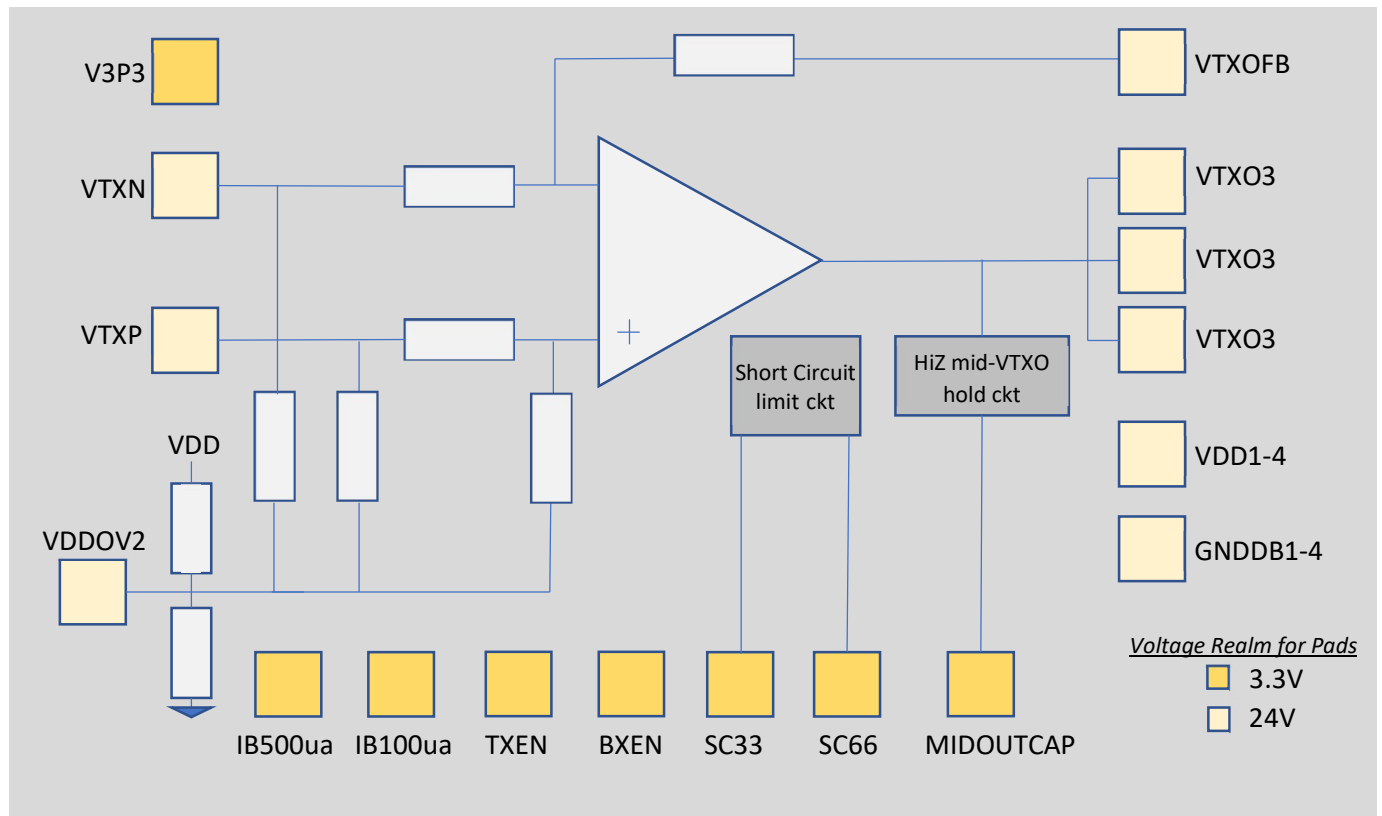
The input is fully differential to allow easy connection to fully differential TX PGA's and filters. Additional resistors are placed on the inputs to add further stability to hold the input voltages steady.

Availability

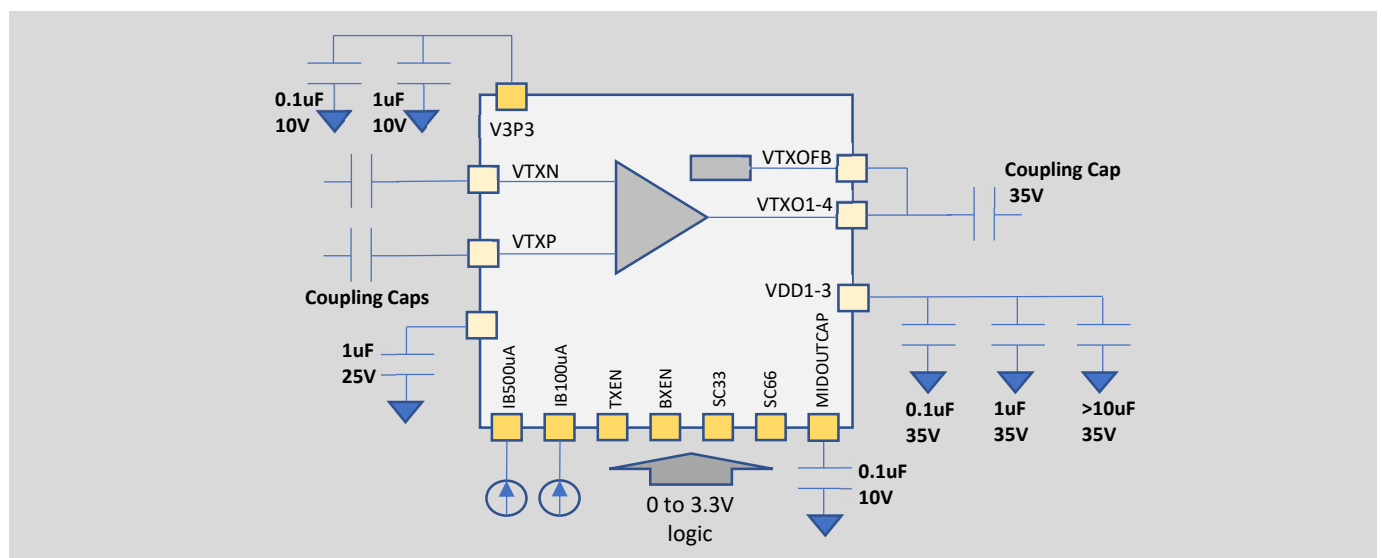
Additional information and demos are available with restrictions. Email: info@plan9inc.com

The IP ownership is offered for sale.

Block Diagram



Application Circuit



Pin Description

Pin Name	Pin on Package	ESD Requirements	Description
MIDOUTCAP	3	5V	Filter for VOTX HiZ circuit, short to disable circuit
SC33	4	5V	LSB Short circuit switch (see decoder)
SC66	5	5V	MSB Short circuit switch (see decoder)
VDDOV2	6	24V	Mid voltage reference cap
VTXP	7	24V	Positive Input
VTXN	8	24V	Negative Input
VDD4	9	24V	VDD supply (in parallel)
VDD3	10	24V	VDD supply (in parallel)
VDD2	11	24V	VDD supply (in parallel)
VDD1	12	24V	VDD supply (in parallel)
VOTX3	13	24V	VOTX output pin (in parallel)
VOTX2	14	24V	VOTX output pin (in parallel)
VOTX1	15	24V	VOTX output pin (in parallel)
VOTXFB	16	24V	VOTX resistor feedback pin (ties to VOTX)
GNDDDB1-4	Paddle	none	Four down bond pads to paddle
TXEN	Internal	5V	Active TX circuit from Standby, H-Active
BXEN	Internal	5V	Activate Standby from Off, H-Active
IB500ua	Internal	5V	Low Variation bias current 500uA
IB100ua	Internal	5V	Low Variation Bias current 125uA

Specifications

Since this is an IP offering, the simulation results are included to show how well the silicon matches simulation. A large amount of agreement between the measured and simulated validates the simulations and that layout minimally impacts the design. Thus, with good agreement, simulations over the corners can be more relied upon to help predict the manufacturing performance limits.

Below are the Overall Conditions for testing, except where noted. The Transmitter was tested over 42 corners comprising of combinations of voltage, temperature, and process corner. In addition, Monte Carlo analysis was employed for certain tests.

Corners used are Typ., FF, SS, FS, SF with various combinations of resistor and capacitor corners.

VDD = 10V and 24V (tested at extreme range, see recommendations)

V3P3 = 3V and 3.6V

Junction Temperature = -40C, 27C, and 150C

Rload= 1 Ohm and 100 Ohms (resistive load)

Cload= 100pF

The actual measurements are in the “Measured” column next to the simulated. These are not exhaustive results over all temperatures but represent the type of performance to be expected.

Absolute Max

Symbol	Description	Conditions	Min	Typ	Max	Units
	VDD		-0.4		24	V
	V3P3 Supply Range		-0.4		5.5	V
	Control pins- SC33, SC66, TXEN, BXEN		-0.4		5.5	V
	VOTX		-0.4		24	V
	Junction Temperature		-40		150	C

Recommended

Symbol	Description	Conditions	Min	Typ	Max	Units
	VDD		10		22	V
	V3P3 Supply Range		3		3.6	V
	Junction Temperature	*depends on application	-40		135*	C

Power Supply Voltages and Currents

Symbol	Description	Conditions	Spec/Sim			Measured			Units
			Min	Typ	Max	Min	Typ	Max	
	VDD Supply Range	Measured at max VDD	10		24	10		24, 20	V
	V3P3 Supply Range		3		3.6	3		3.6	V
	VDD Active Current	No signal (with Plan 9 bias)	45		48		48-50		mA
	VDD Powered Down Current	VDD=24V	240		400		230		uA
	VDD Powered Down Current	VDD=10V					140		uA
	V3P3 Active Current		18		28				uA
	V3P3 Powered Down Current		18		28				uA

Transmitter Inputs

Symbol	Description	Conditions	Spec/Sim			Measured			Units
			Min	Typ	Max	Min	Typ	Max	
	Input Nominal			VDD/2			VDD/2		V
	Input Range (single ended)		0.875* VDD/2		1.125* VDD/2				V
	Input offset Voltage Variation	Input referred	-2.5		2.5	-1		1	mV
	Input Impedance(each)		3.4	4.2	5.1				kOhm

Transmitter Output

Symbol	Description	Conditions	Spec/Sim			Measured			Units
			Min	Typ	Max	Min	Typ	Max	
	Active Output Nominal			VDD/2			VDD/2		V
	Output Range	I _{out} =3A	2		VDD-2		2 to VDD-2		V
	Peak Output Current	SC66=H, SC33=H, Allowable time duration at peak is TBD	3				3		A
	Active Output Voltage	VDD=24V	12.0000		12.000				V
		VDD=15V	2		13	7.497		7.511	V
		VDD=10V				4.995		5.011	V
	Active Output Impedance	At 250kHz *estimated from gain change		<50			8*		mOhm
	HiZ Output Resistance		34		51				kOhm
	HiZ Output Capacitance		61		108				pF
	HiZ Voltage range		0		VDD	0		VDD	V
	HiZ nominal Out Voltage			VDD/2					V
	HiZ nominal Out Voltage	VDD=24V	11.83		12.02				V
		VDD=15V				7.370		7.615	V
		VDD=10V				4.740		5.187	V
	Pside SC Current Limit	SC66=H, SC33=H		3.1			3.2		A
	Pside SC Current Limit	SC66=H, SC33=L		2.7			2.7		A
	Pside SC Current Limit	SC66=L, SC33=H		2.1			2.4		A
	Pside SC Current Limit	SC66=L, SC33=L		1.7			1.9		A
	Nside SC Current Limit	SC66=H, SC33=H		3.2			3.3		A
	Nside SC Current Limit	SC66=H, SC33=L		2.8			3		A
	Nside SC Current Limit	SC66=L, SC33=H		2.2			2.4		A
	Nside SC Current Limit	SC66=L, SC33=L		1.7			1.8		A

Transmitter Bandwidth, Stability, Slew Rate

Symbol	Description	Conditions	Spec/Sim			Measured			Units
			Min	Typ	Max	Min	Typ	Max	
	Gain	100 Ohm load	18.01		18.06		17.97		dB
	Gain	1 Ohm load	18.04		18.08		17.9		dB
	3dB Bandwidth	100 Ohm load	2.26		5.58		3		MHz
	3dB Bandwidth	10 Ohm load					3		MHz
	3dB Bandwidth	1 Ohm load	3.29		7.66		2.7		MHz
	Peaking	100 Ohm load	0		0.044		0		dB
	Peaking	1 Ohm load	0		2		0		dB
	Small Signal Pulse Overshoot	100 Ohm load, VTXO=40mVp	0		0.5		1.6		%
	Small Signal Pulse Overshoot	1 Ohm load, VTXO=40mVp	0		18.7		1.4		%
	Slew Rate Plus	100 Ohm load, 12Vpp (sim'd at 16Vpp), VDD=20V	91.1		161.8		118		V/us
	Slew Rate Negative	same	-159.1		-90.2		-118		V/us
	Full Power Bandwidth	100 Ohm load, 12Vpp, VDD=20V	2.4		4.2		3.1		MHz

Transmitter Noise

Symbol	Description	Conditions	Spec/Sim			Measured			Units
			Min	Typ	Max	Min	Typ	Max	
	Noise Density (input ref)	At 50kHz	16		24.4		-		nV/rtHz
		At 250kHz					17		nV/rtHz
	CEN-A (output ref)	35kHz to 95kHz	31		47		35		uVrms
	CEN-B (output ref)	95k to 125kHz	20		30		25		uVrms
	CEN-C (output ref)	125kHz to 140kHz	14		21		18		uVrms
	CEN-D (output ref)	140kHz to 148kHz	10		15.5		13		uVrms
	ARIB Std-T84 (output ref)	35kHz to 420kHz	68		104		87		uVrms
	FCC-low (output ref)	35kHz to 125kHz	38		56		43		uVrms
	FCC-G3 (output ref)	150kHz to 490kHz	60		94		81		uVrms
	PSRR (VDD) Input Ref	100 Ohm load, @50kHz			-102				dB
	PSRR (VDD) Input Ref	1 Ohm load, @50kHz			-102				dB

Transmitter Distortion

Symbol	Description	Conditions	Spec/Sim			Measured			Units
			Min	Typ	Max	Min	Typ	Max	
	2 nd Harmonic	100 Ohm load, Vout=3Vp, Fund Freq=500kHz	-89		-84		-83		dB
	2 nd Harmonic	10 Ohm load, same					-70		dB
	2 nd Harmonic	1 Ohm load, same	-100		-64		-53		dB
	3 rd Harmonic	100 Ohm load, same	-100		-80		-88		dB
	3 rd Harmonic	10 Ohm load, same					-69		dB
	3 rd Harmonic	1 Ohm load, same	-77		-54		-55		dB
	MTPR Average Bin	100 Ohm load, 3Vp, CF=4, 260 tones (appx 9k to 480kHz) Fund freq=488.28125Hz	72		83		90		dB
	MTPR Average Bin	10 Ohm load, same as above					90		dB
	MTPR Average Bin	1 Ohm load, same as above	51		65		71		dB
	MTPR Peak Bin	100 Ohm load, same as above	54		71		77		dB
	MTPR Peak Bin	10 Ohm load, same as above					75		dB
	MTPR Peak Bin	1 Ohm load, same as above	40		57		58		dB

Die Area

Transmitter size, without bond pads and ESD, is 1400x890um = 1.246mm²

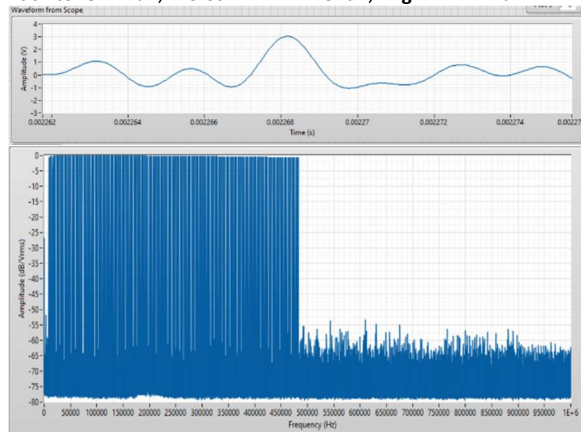
Measurement Results

MTPR

Typical Measurement result of MTPR signal with 260 tones producing peaks of 3V while driving a 1 Ohm load with VDD= 10V, is shown below. The peak current is 3A with the average current about 300mA. This measurement uses tones and empty bins evenly spaced. Intermodulation distortion collects in the empty bins and is compared to the signal, with both an average MTPR S/N and a worst-case bin calculation. All dB calculations are in Volts.

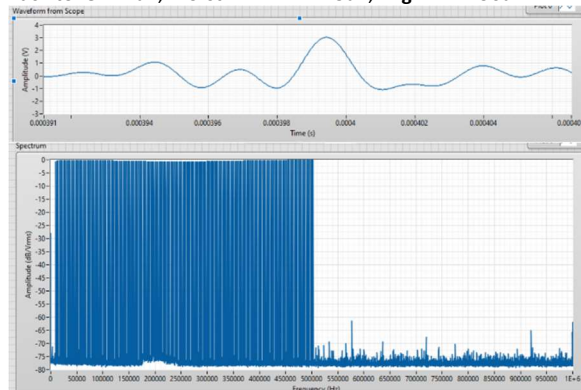
Load=1 Ω , VDD=10V or VDD=15V

Each tone: -24dB, Worst Bin MTPR: 57dB, Avg MTPR: 71dB



Load=10 Ω

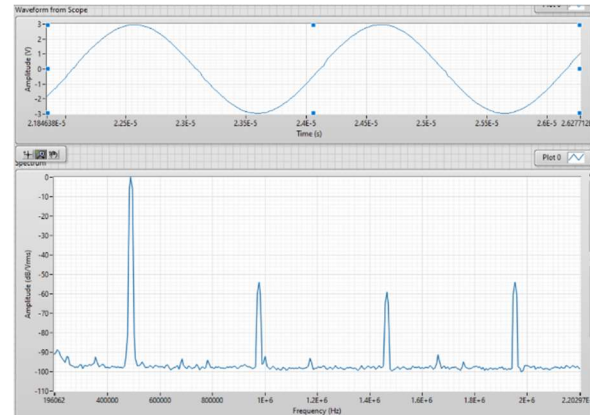
Each tone: -24dB, Worst Bin MTPR: 75dB, Avg MTPR: 90dB



Harmonic Distortion

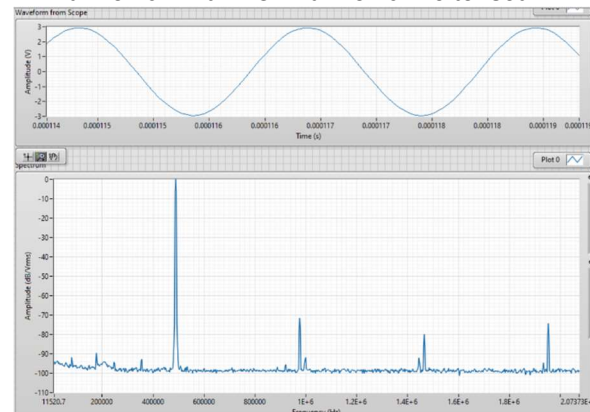
Vout = 6Vpp, Load= 1 Ω , VDD=10V or 15V

2nd Harmonic: -54dB 3rd Harmonic: -60 to -55dB



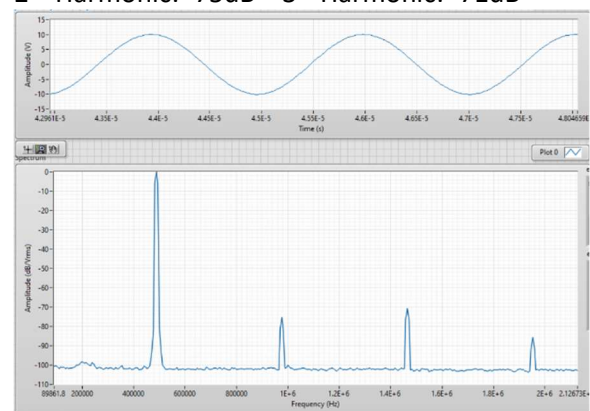
Vout = 6Vpp, Load= 10 Ω , VDD= 10 or 15V

2nd Harmonic: -72dB 3rd Harmonic: -70 to -80dB



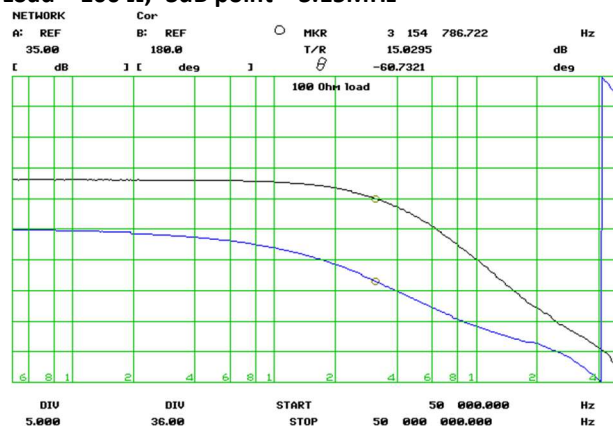
Vout = 20.5Vpp, Load= 50 Ω , VDD=21V

2nd Harmonic: -75dB 3rd Harmonic: -71dB

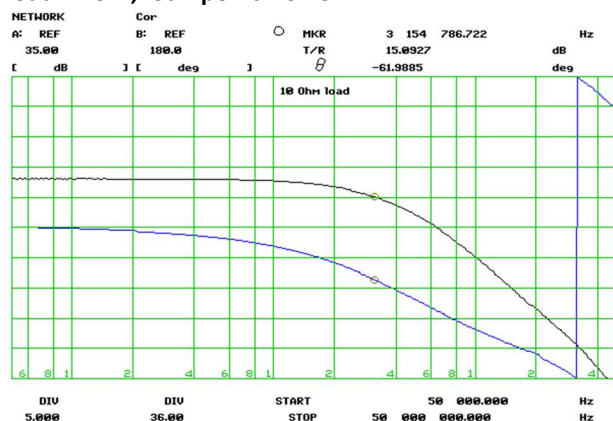


Bode Plot

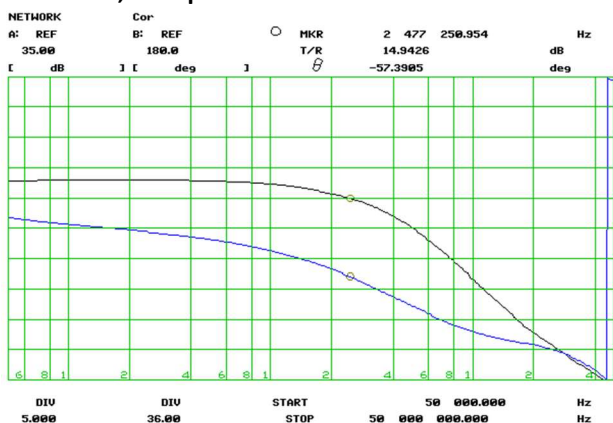
Load = 100 Ω , -3dB point = 3.15MHz



Load = 10 Ω , -3dB point = 3.15MHz

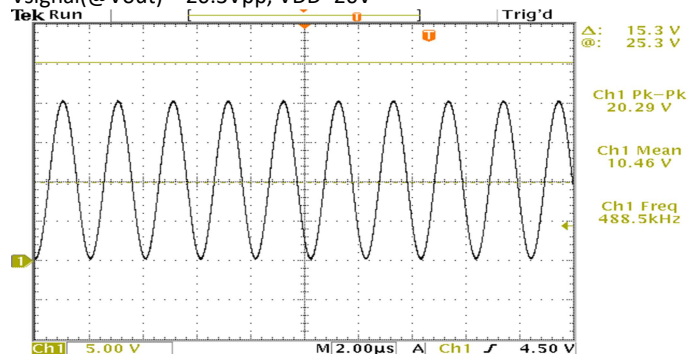


Load = 1 Ω , -3dB point = 2.5MHz



Signal driving Output during HiZ

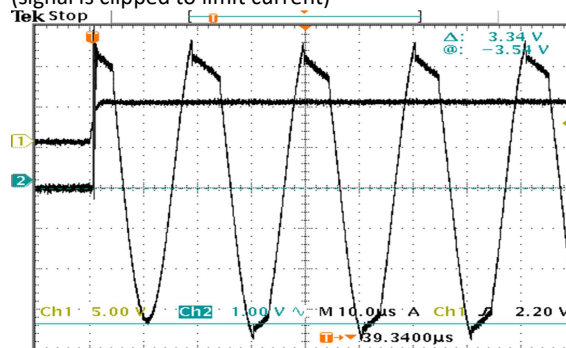
Vsignal(@Vout) = 20.3Vpp, VDD=20V



Short Circuit Protection 3.2A

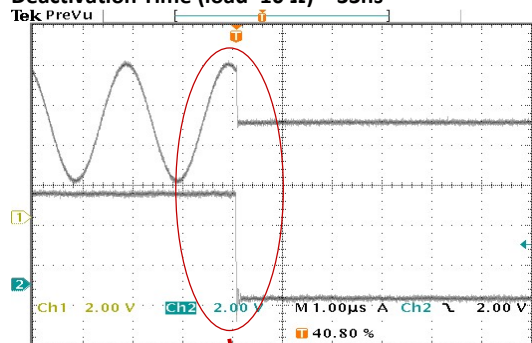
Set to 3.2A current limit VDD=10V

(signal is clipped to limit current)

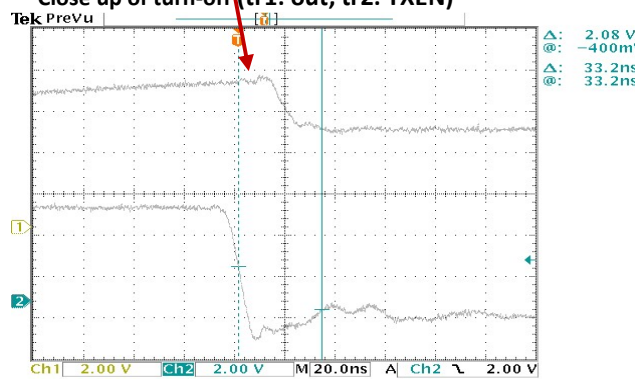


Output deactivating and going to HiZ mode

Deactivation Time (load=10 Ω) = 33ns

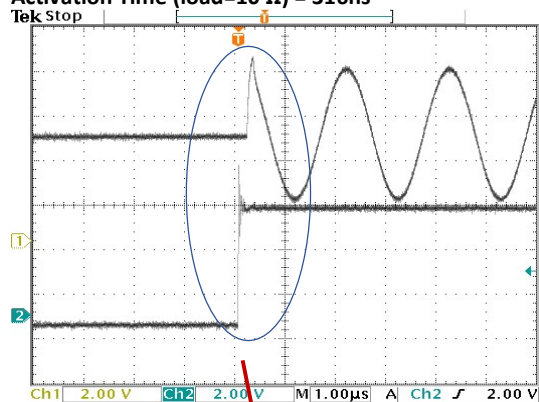


Close up of turn-off (tr1: out, tr2: TXEN)



Output activation and driving signal

Activation Time (load=10 Ω) = 316ns



Close up of turn-on (tr1: out, tr2: TXEN)

