P1000 TX Application Circuit Description: Power Dissipation

Don Whitney
Plan 9, Inc.
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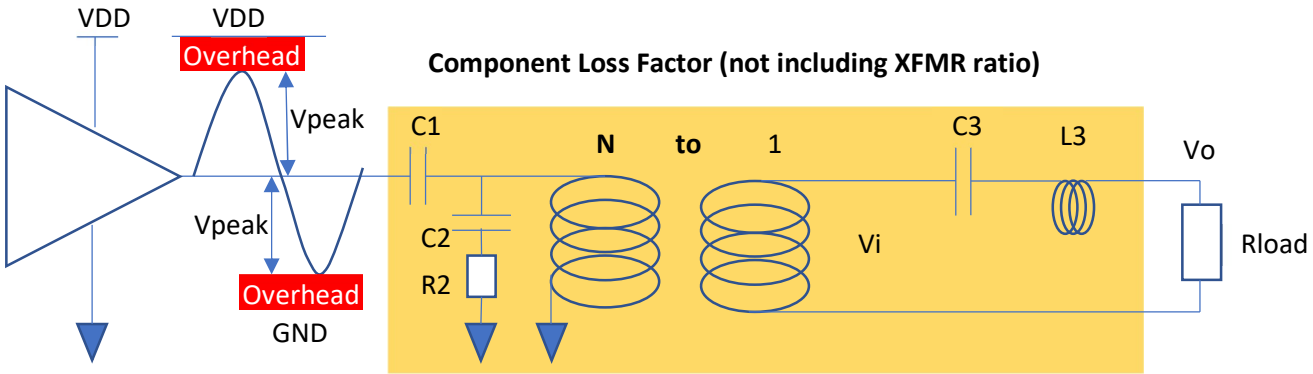
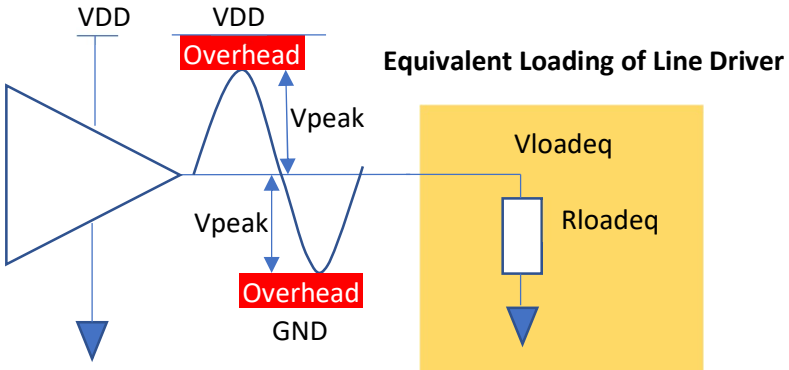
Various parameters can affect the performance of the narrow band Power Line Communications channel. Properly understanding and optimizing these parameters will lead to a high performing, robust system with minimum tradeoffs. This application report will discuss power dissipation, die temperature, and overhead voltage which are crucial for reliable system. Below is a schematic of the system with the interface circuitry including a transformer coupling. If the entire application circuit was replaced with just an equivalent load it would look like the next picture. This simplified model will make the analysis easier but remember that the Rloadeq depends on the transformer ratio, the Rload, and rest of the components.



Circuit with the equivalent load.



Power Dissipation

The power and the system's ability to dissipate it determine the internal die temperature. The internal die temperature often has a limit on what it can be before there is potential performance degradation or a shutdown of the circuit. Also, long term reliability is affected by the die temperature over time.

To calculate the power dissipation of the line driver, there are several steps. They are:

1) Calculate the RMS current in the equivalent load
2) Use the load current to calculate the average current from the VDD supply
3) Using the average current from the supply and the VDD supply voltage to calculate the power dissipation which includes the load.
4) Calculate the power dissipated of the load
5) Subtract the load power from the total power to calculate the actual power dissipation of the chip
6) From here the die temperature rise could be calculated.

Definition of calculating the RMS for a continuous waveform

$$VLoadeq\_rms = \sqrt{\frac{1}{T1 - T0} * \int_{T0}^{T1} (Vwaveform(t))^2 \, dt}$$

Modified for a discrete sampling

$$Vloadeq\_rms = \sqrt{\frac{1}{T1 - T0} * \sum_{t=T0}^{T1} (Vwaveform(t))^2}$$

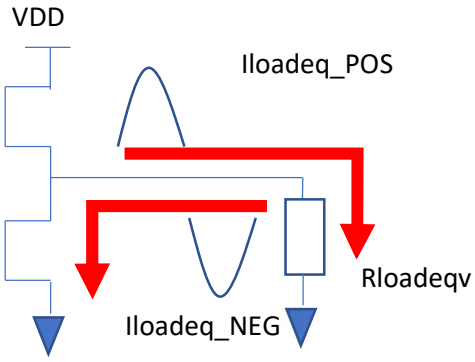
$$ILoadeq\_rms = \frac{1}{RLoadeq} * \sqrt{\frac{1}{T1 - T0} * \sum_{t=T0}^{T1} (Vloadwaveform(t))^2}$$

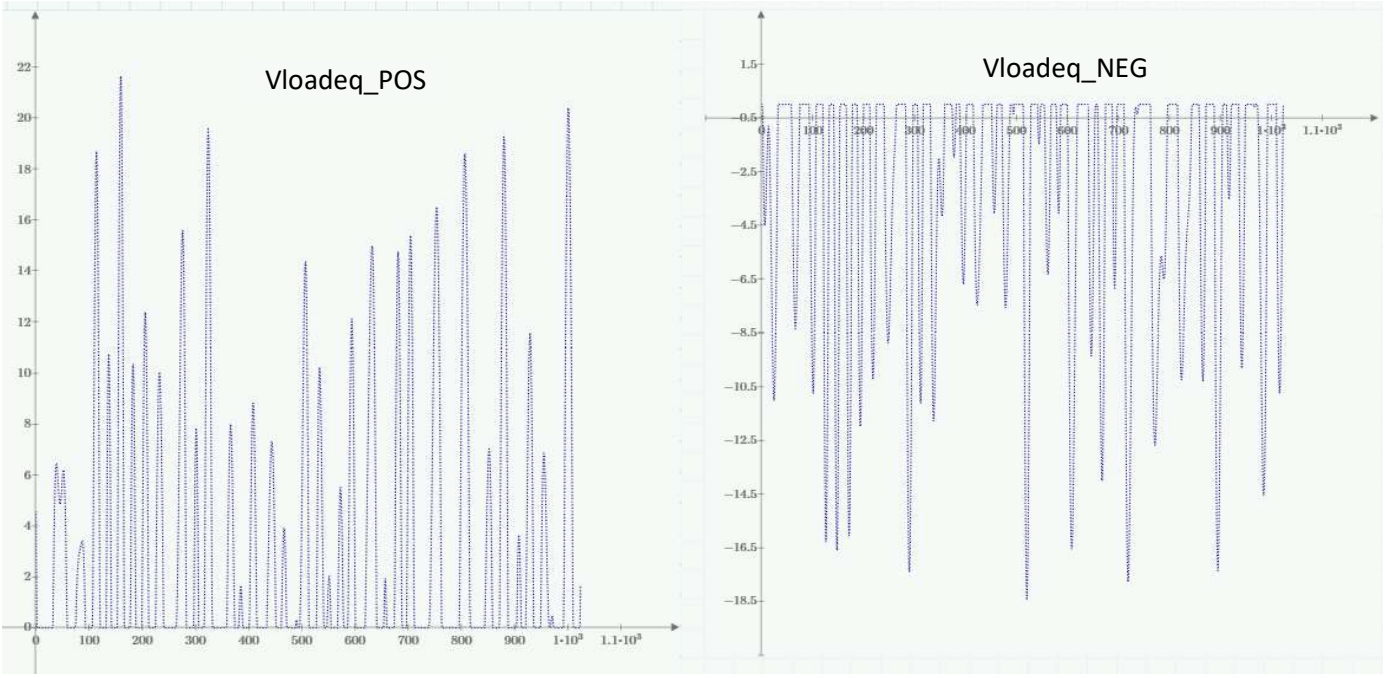
Where:
T1-T0 is the period of the fundamental frequency

Vwaveform(t) is the signal as function of time. In this example, the Vwaveform(t) is considered an OFDM multitone waveform with tones from 9kHz to 500kHz with tones with spacing of 488.28125Hz (1/2.048 ms).

Determine the Average current from the Power Supply

The next step is to find the average current from the power supply as a function of the rms load current. With a single output line driver, the current from VDD occurs only during the positive cycle and during the other cycle the current goes to ground and has no VDD current; however, it adds to the power dissipation of the line driver. Thus, only the positive half of the signal of the load current should be used.





To create a clipped signal, a function could be written to extract the positive or negative half of the load current (this is not to scale). Alternatively, absolute value of the function will clip the signal, but it combines the positive and negative cycles.

$$Iavg2x = \frac{1}{T1 - T0} * \sum_{t=T0}^{T1} |Iwaveform(t)|$$

However, most signals are eventually symmetrical over time which is simulation has backed up, thus both halves (POS and NEG) are considered to have equal average magnitude. Thus, the above equation can just be divided in two to represent the current from VDD.

$$IVDDavg = \frac{1}{T1 - T0} * \frac{1}{2} * \sum_{t=T0}^{T1} |Iwaveform(t)|$$

Ratioing the IVDDavg and Iloadrms equations to calculate a factor that can be used to calculate the IVDDavg from the Iloadrms value.

$$\frac{IVDDavg}{Iloadrms} = \frac{\frac{1}{T1-T0} * \frac{1}{2} * \sum_{t=T0}^{T1} |Iwaveform(t)|}{\sqrt{\frac{1}{T1-T0} * \sum_{t=T0}^{T1} \left(Iwaveform(t)\right)^2}} = \frac{\frac{1}{T1-T0} * \frac{1}{2} * \sum_{t=T0}^{T1} |Iwaveform(t)|}{\frac{1}{Rloadeq} * \sqrt{\frac{1}{T1-T0} * \sum_{t=T0}^{T1} \left(Vwaveform(t)\right)^2}}$$

Using a Sinewave signal as the Iwaveform and performing the above calculation with a script, the ratio is **0.45** (sqrt(2)/pi) which is half of the textbook ratio (2*sqrt(2))/pi because only half of the waveform is being used for the average. This test agrees with theory.

Using the above OFDM signal for Iwaveform and solving with a script, the ratio of Average(half)/RMS is **0.4** which is a little less than the sinewave.

$$\frac{IVDDavg}{Iloadeqrms} = 0.4$$

Now the total power of the chip and load can be calculated.

Power Calculation

During the normal line driver operation, current flows from VDD to the load through the upper line driver output device (PMOS) during the positive cycle and then the current comes from the load to ground through the lower line driver output device (NMOS). Even though current is drawn from VDD only during the positive half of the cycle both cycles contribute to the power dissipation of the chip since the NMOS dissipates power during the sinking of the negative cycle. Conceptionally, it might be better to divide the cycles in two parts and to divide the power supply into two parts also, such that each half cycle includes IVDDavg (assuming the magnitude of both halves are equal) and only VDD/2 since each half cycle occurs within VDD/2.

$$PowerTotal = PowerPoshalf + PowerNeghalf$$

$$PowerTotal = \frac{VDD}{2} * IVDDavg + \frac{VDD}{2} * IVDDavg = VDD * IVDDavg$$

Using the above relationship, then

$$PowerTotal = VDD * Iloadeqrms * 0.4$$

The value above includes the power delivered to the load. To extract just the power dissipation of the line driver, the loadeq power should be subtracted from the total power.

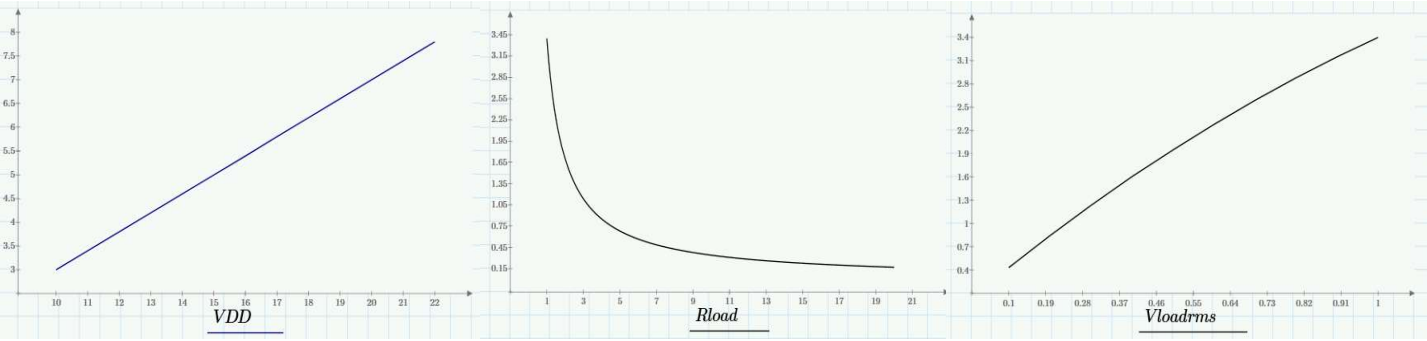
$$PowerTotalLD = VDD * Iloadeqrms * 0.4 - Iloadeqrms^2 * Rloadeq = VDD * \frac{Vloadeqrms}{Rloadeq} * 0.4 - \frac{Vloadeqrms^2}{Rloadeq}$$

The chip itself will have some amount of quiescent power (Pq) represents the rest of the circuitry. The advertised quiescent current includes the class A current of the AB stage when the amplifier is idling. When the amplifier is transmitting a high current signal, the Pq from the output is accounted for from the output current and a rule of thumb value is to use something around 60-70% of the datasheet current to calculate the added quiescent power.

$$PowerTotalLDQ = VDD * Iloadrms * 0.4 - Iloadrms^2 * Rload = VDD * \frac{Vloadrms}{Rload} * 0.4 - \frac{Vloadrms^2}{Rload} + Pq$$

From the equation and below graphs, it can be discerned that increasing VDD adds power, increasing the load resistance lowers the power, and increasing the Load signal level increase power. However, there are various tradeoffs to be made to optimize these that will be discussed in the next application note.

The Y Axis of all three is Power in Watts.



The above analysis provides the ability to estimate the power generation of the line driver based on various variables. The power estimates can be used to determine how much the die temperature will rise. The die temperature is important to reliability and operation of the chip is dependent on the power generation and the ability to dissipate the heat.

Temperature Rise

A simple way of looking at complex temperature change in the chip is to use a calculated, estimated, or simulated Theta JA which relates the chip die power to a rise in junction temperature relative to the ambient temperature. The Theta JA represents how well the chip, package, board, and enclosure can remove the heat. The smaller the Theta JA, the better. For instance, an estimated Theta JA of the 44 Pin QFN with a pad, highly metalized four-layer board, and reasonable enclosure is about 17C/Watt. If the chip from the above equation dissipates power, then the die temperature will rise the following amount.

$$TemperatureDieRise = ThetaJA * PowerTotalLDQ$$

When related to the ambient temperature, the actual die temperature can be calculated.

$$TemperatureDie = AmbientTemp + ThetaJA * PowerTotalLDQ$$

The typical ambient maximum temperature for the board/chip within an enclosure is 70C commercial and 85C industrial. The die temperature is often limited to 135C or 150C (the P1000/P2000 have been designed to operate at 150C). Thus, at 85C, the maximum increase of temperature is 50C or 65C which limits the dissipation of the line driver to

$$Power\ dissipation\ Max = \frac{TempDie - AmbientTemp}{ThetaJA} = \frac{135 - 85}{17} = 3W$$

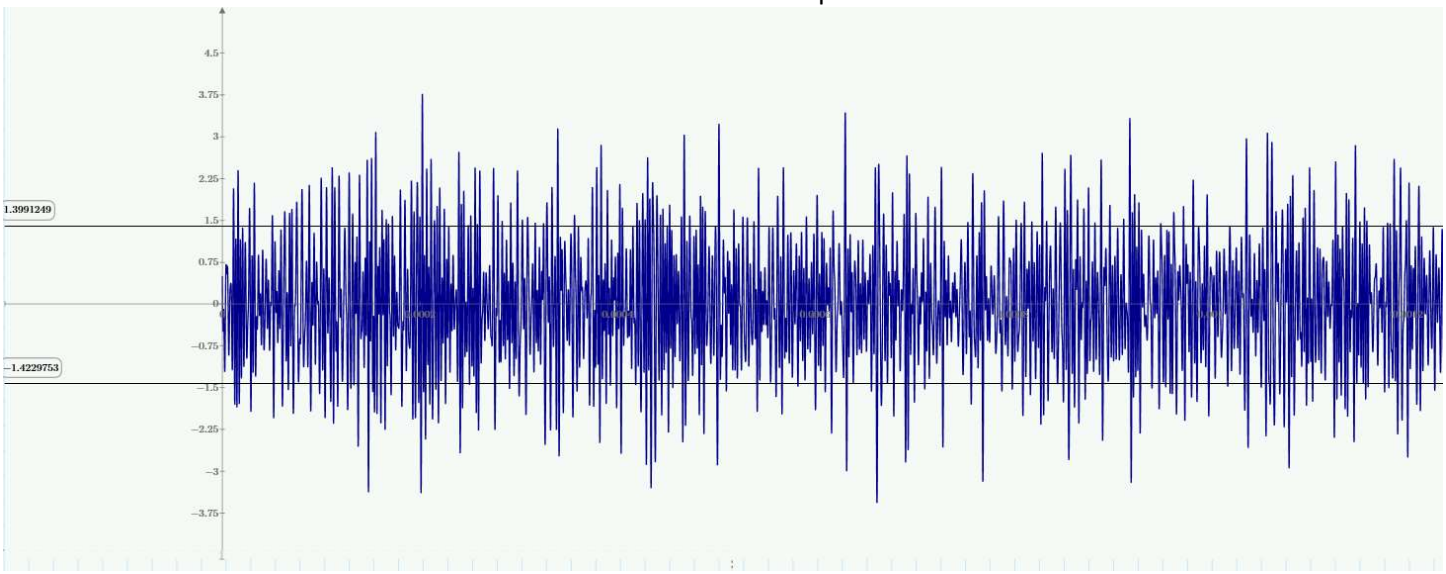
Or at the higher die temperature,

$$Power\ dissipation\ Max = \frac{TempDie - AmbientTemp}{ThetaJA} = \frac{150 - 85}{17} = 3.8W$$

Overhead Voltage and VDD

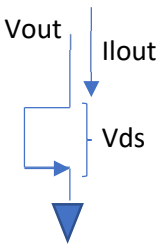
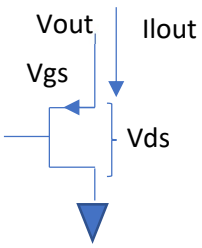
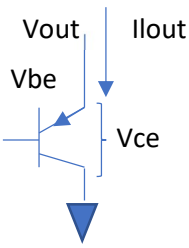
OFDM signals are great to transmit a lot of information, but with one flaw that the analog designer gets to deal with, that is the Peak to RMS or Crest Factor (CF) is much higher that of a sinewave (1.41) and could be as high as 4.5. The analog signal processing chain and the line driver circuit must accommodate not only the RMS signal voltage, but the CF also. If the rms value is 1Vrms then the peak value can be 3.5Vp if the CF=3.5. Thus, the VDD voltage must be adjusted for this additional overhead voltage.

1V RMS OFDM with CF=3.75 The horizontal markers show what the peak would be for a sinewave.



Amplifier Overhead

Amplifier output stages require some additional overhead to allow for proper operation. Most output stage configurations are either common source, source follower, or Emitter followers. Each requires some amount of voltage backoff depending on the operating conditions. The P1000/P2000 are Common Source.

Configuration	Common Source	Source Follower	Emitter Follower
Schematic Representation			
What limits Vo swing towards the rails	Vds	Vgs+Vds	Vbe+Vce
Voltage Overhead needed Amount (approximate) under load	P1000 Vds=0.67*Ilout Vds=2V min @ 3A	Vgs= 1.5-3V when Iload is high Vds=1-4V depending on load	Vbe= 0.7-1.1V when Iload is high Vce=1-4V depending on load
Voltage Overhead needed without load	Rail to Rail with no load	Vgs	Vbe

For example, the Vrms= 1V, the CF=3.5, and the overhead voltage is 2V for each rail. The total Peak to Peak swing of the line driver is (units in red)

$$Vrms * CF * 2 = 1(Vrms) * 3.5(\frac{Vp}{Vrms}) * 2(\frac{Vpp}{Vp}) = 7Vpp$$

Add the overhead to the VDD and Gnd sides,

$$VDDmin = 1(Vrms) * 3.5\left(\frac{Vp}{Vrms}\right) * 2\left(\frac{Vpp}{Vp}\right) + 2V + 2V = 11Vpp = 11V$$

Thus, the minimum VDD power supply would be 11V. If this were just a sinewave, then the minimum VDD would be

$$VDDmin = Vrms * CF * 2 + Voverhead * 2 = 1(Vrms) * 1.414(\frac{Vp}{Vrms}) * 2(\frac{Vpp}{Vp}) = 6.8V$$

The P1000 has one of the lowest overhead voltages because of the large output devices and that it is configured with a common source output stage. Those that use other configurations have much higher overhead voltages which increases the VDD and thus increases the power.

However, this is based on what the demands of the Rloadeq which includes the transformer. The transformer ratio can be used to trade off voltage for current by to optimizing VDD, line driver signal levels, current loads, etc. to achieve the signal on the line goals and minimize the power dissipation of the line driver. This will be the topic of the next application note, so stay tuned for the next installment.