The P2000 line driver is an improved version of the P1000 line driver. The P2000 also is a Power Line Communications (PLC) Narrow Band (9-500kHz) Transmitter line driver block and designed to drive the low impedance loads with outstanding linearity and MTPR (Multi-Tone Power Ratio) performance driving OFDM signals.

Improvements include:

- *Stable with 2nFd capacitor load*
- *Greater tolerance of load inductance during short circuit*
- *Improved short circuit performance*
- *Additional circuitry to enable smarter transmission control*

Applications include:

- *All PLC related standards*
- *Smart power meter communications*
- *Smart House controls*

Features of this IP Transmitter:

- *3 Amp output @ VDD-2V*
- *>500KHz Full Power Bandwidth*
- *Fully Differential Input and Single ended Output*
- *Switchable hi-impedance output mode*
- *Fixed Gain of 8V/V*
- *<50mA idle current*
- *VDD range is 10V to 24V*
- *Programmable Short circuit Protection*
- *HiZ output holding circuit*
- *Is stable directly driving up to a 2nF capacitive load*
- *IP line driver total area is less than 1.32mm2*

Description

The AC power line was not intended for data transmission. High voltage, current spikes, induced noise, switching noise, low impedance loads, impedance nulls, and lossy transmission all challenge a communication channel and the frontline AFE components but especially the line driver. The Plan 9 line-driver was designed to better meet these challenges.

The line driver can drive low impedance loads at high current and still maintain the low distortion needed for OFDM signals. The ability to drive 2nF capacitor load directly and without any other load, removes the need for current reducing series resistors to maintain stability.

The short circuit current limit clips the fast-moving signal (up to 500KHz) in efforts to minimize fidelity issues during transmission of difficult loads. There are four choices of short circuit current.

During the output HiZ mode, the midpoint can sometimes drift from the active midpoint causing transients and filter settling times during re-activation of the line driver. A mid-point hold circuit is used to keep the voltage during HiZ mode but not lower the open impedance at working frequencies.

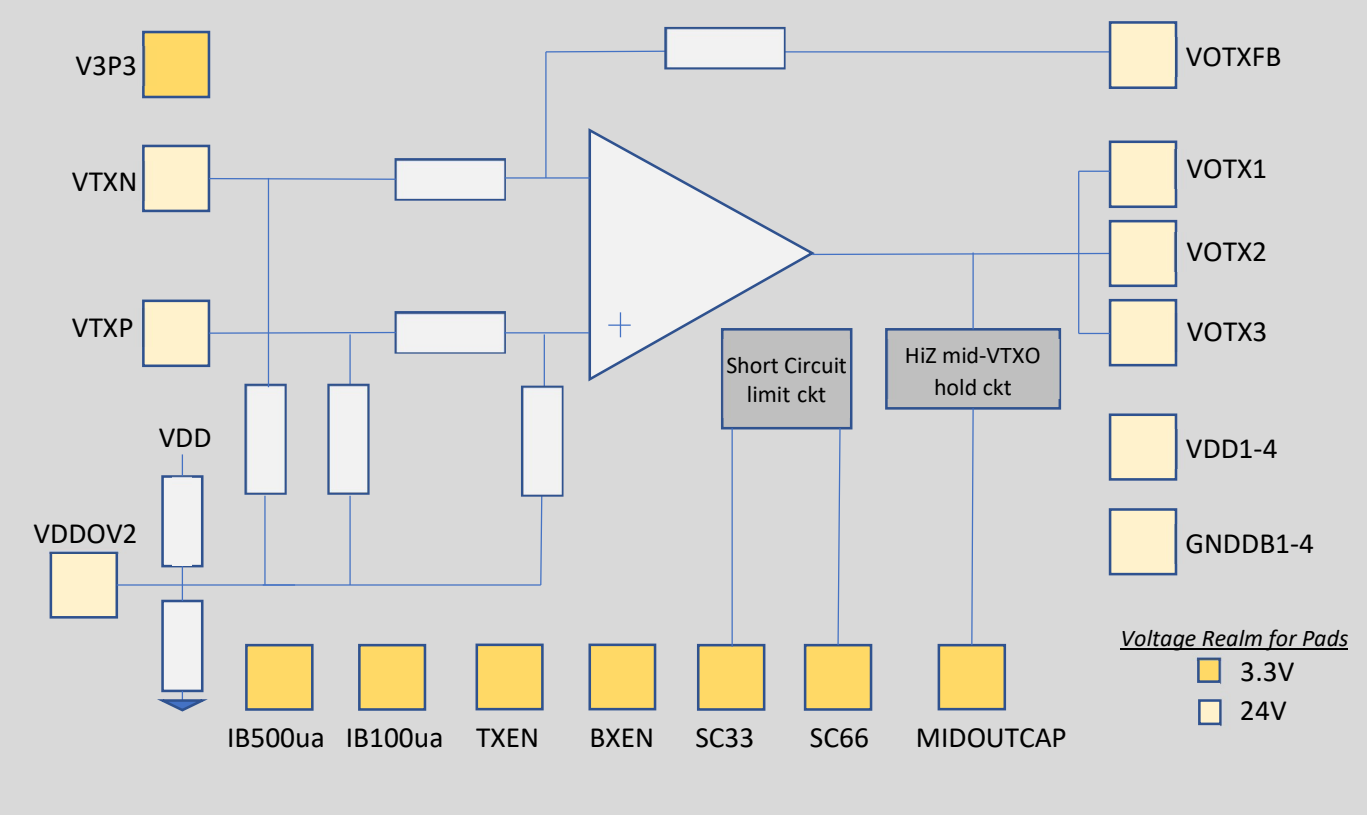
The input is fully differential to allow easy connection to fully differential TX PGA's and filters. Additional resistors placed on the inputs to add further stability to hold the input voltages steady.

Availability

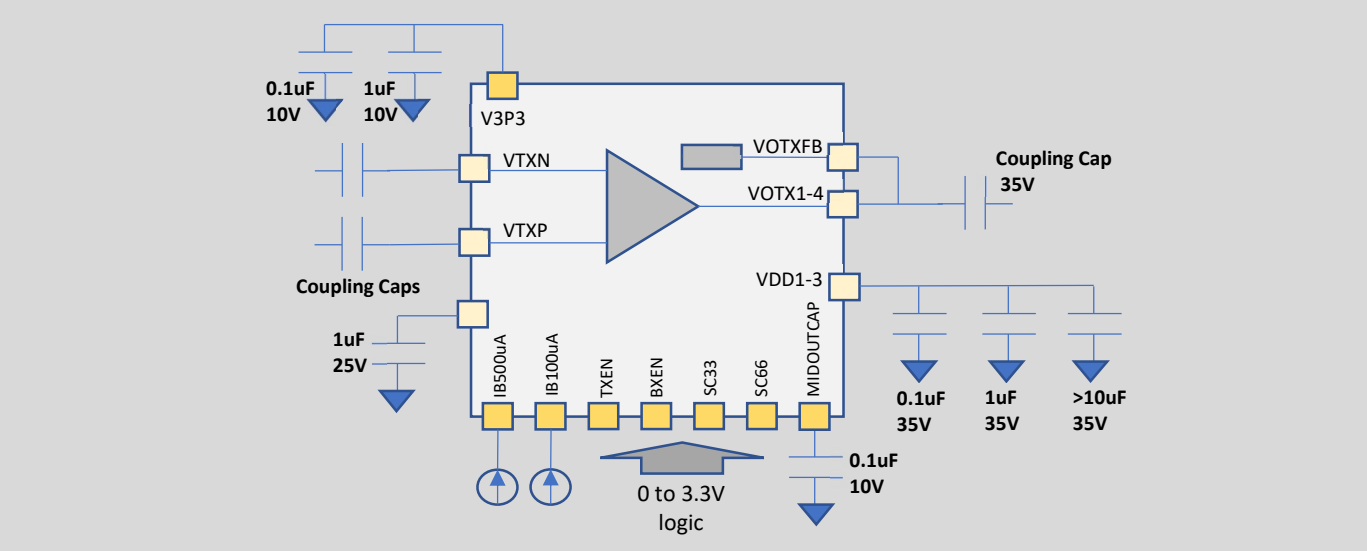
Additional information and demos are available with restrictions. Email: info@plan9inc.com

The IP ownership is offered for sale.

Block Diagram



Application Circuit



Pin Description

Pin Name	Pin on Package	ESD Requirements	Description
MIDOUTCAP	3	5V	Filter for VOTX HiZ circuit, short to disable circuit
SC33	4	5V	LSB Short circuit switch (see decoder)
SC66	5	5V	MSB Short circuit switch (see decoder)
VDDOV2	6	24V	Mid voltage reference cap
VTXP	7	24V	Positive Input
VTXN	8	24V	Negative Input
VDD4	9	24V	VDD supply (in parallel)
VDD3	10	24V	VDD supply (in parallel)
VDD2	11	24V	VDD supply (in parallel)
VDD1	12	24V	VDD supply (in parallel)
VOTX3	13	24V	VOTX output pin (in parallel)
VOTX2	14	24V	VOTX output pin (in parallel)
VOTX1	15	24V	VOTX output pin (in parallel)
VOTXFB	16	24V	VOTX resistor feedback pin (ties to VOTX)
GNDDB1-4	Paddle	none	Four down bond pads to paddle
TXEN	18	5V	Active TX circuit from Standby, H-Active
BXEN	28	5V	Activate Standby from Off, H-Active
IB500ua	Internal	5V	Low Variation bias current 500uA
IB100ua	Internal	5V	Low Variation Bias current 125uA

Specifications

Only simulation results are included at this time. The silicon of the P1000 demonstrated a large amount of agreement between the measured and simulated which validates the simulations and that layout minimally impacts the design. So, the P2000 is expected to has the same close correlation between silicon results and simulations. Thus, with good agreement, simulations over the corners can be more relied upon to help predict the manufacturing performance limits.

Below are the Overall Conditions for testing, except where noted. The Transmitter was evaluated at over 42 corners comprising of combinations of voltage, temperature, and process corner. In addition, Monte Carlo analysis was employed for certain tests.

Corners used are Typ., FF, SS, FS, SF with various combinations of resistor and capacitor corners.

VDD = 10V and 24V (evaluated at extreme range, see recommendations)
V3P3 = 3V and 3.6V
Junction Temperature = -40C, 27C, and 150C
Rload= 1 Ohm and 100 Ohms (resistive load)
Cload= 0 or **2nF**

Absolute Max

Symbol	Description	Conditions	Min	Typ	Max	Units
	VDD		-0.4		24	V
	V3P3 Supply Range		-0.4		5.5	V
	Control pins- SC33, SC66, TXEN, BXEN		-0.4		5.5	V
	VOTX		-0.4		24	V
	Junction Temperature		-40		150	C

Recommended

Symbol	Description	Conditions	Min	Typ	Max	Units
	VDD		10		22	V
	V3P3 Supply Range		3		3.6	V
	Junction Temperature	*depends on application	-40		135*	C

Power Supply Voltages and Currents

			P1000 Spec/Sim			P2000 Spec/Sim			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	VDD Supply Range	Measured at max VDD	10		24	10		24, 20	V
	V3P3 Supply Range		3		3.6	3		3.6	V
	VDD Active Current	No signal (with Plan 9 bias)	45		48	47		50	mA
	VDD Powered Down Current	VDD=24V	240		400	247		431	uA
	VDD Powered Down Current	VDD=10V							uA
	V3P3 Active Current					520		540	uA
	V3P3 Powered Down Current		18		28	18		28	uA

Transmitter Inputs

			P1000 Spec/Sim			P2000 Spec/Sim			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Input Nominal			VDD/2			VDD/2		V
	Input Range (single ended)		0.875* VDD/2		1.125* VDD/2	0.875* VDD/2		1.125* VDD/2	V
	Input offset Voltage Variation	Input referred	-2.5		2.5	-2.5		2.5	mV
	Input Impedance(each)		3.4	4.2	5.1	3.4	4.2	5.1	kOhm

Transmitter Output

			P1000 Spec/Sim			P2000 Spec/Sim			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Active Output Nominal			VDD/2			VDD/2		V
	Output Range	Iout=3A	2		VDD-2		2 to VDD-2		V
	Peak Output Current	SC66=H, SC33=H, Allowable time duration at peak is TBD	3				3		A
	Active Output Voltage	VDD=24V VDD=15V VDD=10V	12.0000		12.000	12		12.0003	V V V
	Active Output Impedance	At 250kHz *estimated from gain change		<50			8*		mOhm
	HiZ Output Resistance		34		51	22		49.5	kOhm
	HiZ Output Capacitance		61		108	92		155	pF
	HiZ Voltage range		0		VDD	0		VDD	V
	HiZ nominal Out Voltage			VDD/2					V
	HiZ nominal Out Voltage	VDD=24V VDD=15V VDD=10V	11.83		12.02	11.9998		12.00562	V V V
	Pside SC Current Limit	SC66=H, SC33=H		3.1		3.15		3.55	A
	Pside SC Current Limit	SC66=H, SC33=L		2.7		2.58		2.72	A
	Pside SC Current Limit	SC66=L, SC33=H		2.1		2.12		2.21	A
	Pside SC Current Limit	SC66=L, SC33=L		1.7		1.79		1.86	A
	Nside SC Current Limit	SC66=H, SC33=H		3.2		3.08		3.62	A
	Nside SC Current Limit	SC66=H, SC33=L		2.8		2.58		2.73	A
	Nside SC Current Limit	SC66=L, SC33=H		2.2		2.10		2.19	A
	Nside SC Current Limit	SC66=L, SC33=L		1.7		1.76		1.82	A

Transmitter Bandwidth, Stability, Slew Rate

			P1000 Spec/Sim			P2000 Spec/Sim			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Gain	100 Ohm load	18.01		18.06	17.99		18.05	dB
	Gain	1 Ohm load	18.04		18.08	18.04		18.08	dB
	3dB Bandwidth	100 Ohm load	2.26		5.58	1.9		4.9	MHz
	3dB Bandwidth	10 Ohm load				2		5.1	MHz
	3dB Bandwidth	1 Ohm load	3.29		7.66	2.6		6.9	MHz
	Peaking	100 Ohm load	0		0.044	0		0	dB
	Peaking	1 Ohm load	0		2	0		1	dB
	Small Signal Pulse Overshoot	100 Ohm, 2nF load, VTXO=40mVp	0		0.5	0		0	%
	Small Signal Pulse Overshoot	1 Ohm, 2nF load VTXO=40mVp	0		18.7	0		11	%
	Slew Rate Plus	100 Ohm load, 12Vpp (sim'd at 16Vpp), VDD=20V	91.1		161.8	62		96	V/us
	Slew Rate Negative	same	-159.1		-90.2	-96		-62	V/us
	Full Power Bandwidth	100 Ohm load, 12Vpp, VDD=20V	2.4		4.2	1.6		2.6	MHz

Transmitter Noise

			P1000 Spec/Sim			P2000 Spec/Sim			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Noise Density (input ref)	At 50KHz	16		24.4	18		26	nV/rtHz
	CEN-A (output ref)	35kHz to 95kHz	31		47	34		49.6	uVrms
	CEN-B (output ref)	95k to 125kHz	20		30	21		31.6	uVrms
	CEN-C (output ref)	125kHz to 140kHz	14		21	14.4		21.8	uVrms
	CEN-D (output ref)	140kHz to 148kHz	10		15.5	10.4		15.8	uVrms
	ARIB Std-T84 (output ref)	35kHz to 420kHz	68		104	71.3		108.5	uVrms
	FCC-low (output ref)	35kHz to 125kHz	38		56	40.1		59	uVrms
	FCC-G3 (output ref)	150kHz to 490kHz	60		94	62		96.7	uVrms
	PSRR (VDD) Input Ref	100 Ohm load, @50kHz			-102			-101	dB
	PSRR (VDD) Input Ref	1 Ohm load, @50kHz			-102				dB

Transmitter Distortion

			P1000 Spec/Sim			P2000 Spec/Sim			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
		1000 Ohm load, Vout=3Vp, Fund Freq=500kHz P1000- 200pF, P2000- 2nF				-102		-81	dB
	2nd Harmonic	100 Ohm load	-89		-84	-93		-80	dB
	2nd Harmonic	10 Ohm load, same				-91		-73	dB
	2nd Harmonic	1 Ohm load, same	-100		-64	-88		-66	dB
	3rd Harmonic	1000 Ohm load, same				-101		-79	dB
	3rd Harmonic	100 Ohm load, same	-100		-80	-104		-79	dB
	3rd Harmonic	10 Ohm load, same				-73		-55	dB
	3rd Harmonic	1 Ohm load, same	-77		-54	-66		-48	dB
	MTPR Average Bin	**1k Ohm/2nF** load, 3Vp, CF=4, 260 tones (appx 9k to 480kHz) Fund freq=488.28125Hz				79		83	dB
	MTPR Average Bin	100 Ohm/200pfd load, same	72		83				
	MTPR Average Bin	1 Ohm/2nF or 200p load, same as above	51		65	52		64	dB
	MTPR Peak Bin	**1k Ohm/2nF** load, same as above				70		75	dB
	MTPR Peak Bin	100 Ohm load, same as above	54		71				dB
	MTPR Peak Bin	1 Ohm load, same as above	40		57	43		56	dB

Die Area

Transmitter size, without bond pads and ESD, is 1480x890um = 1.32mm2

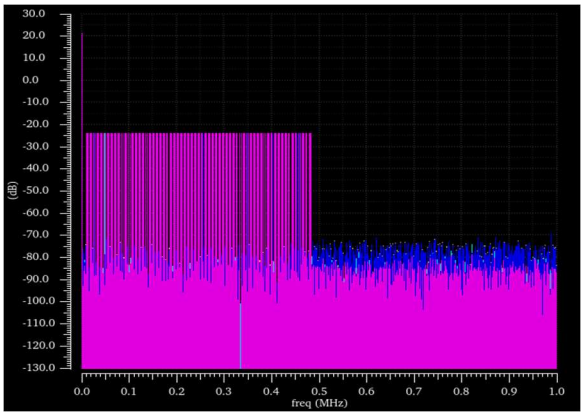
Measurement Results

MTPR

Typical Measurement result of MTPR signal with 260 tones producing peaks of 3V while driving a 1 Ohm load with VDD= 10V, is shown below. The peak current is 3A with the average current about 300mA. This measurement uses tones and empty bins evenly spaced. Intermodulation distortion collects in the empty bins and this noise/distortion is ratioed to the signal, with both an average MTPR S/N and a worst-case bin calculation. All dB calculations are in Volts.

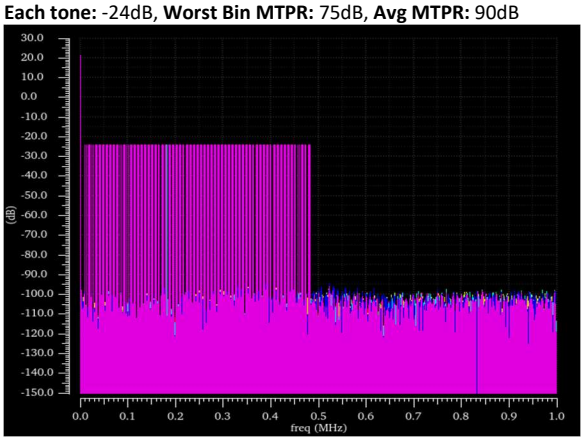
Load=2nF, 1 Ω, VDD=10V

Each tone: -24dB, **Worst Bin MTPR:** 43-56dB, **Avg MTPR:** 52-64dB



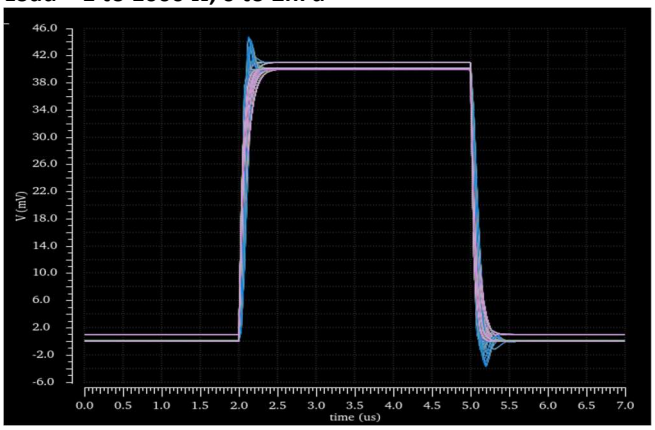
Load=2nF, 1000 Ω, VDD=10V

Each tone: -24dB, **Worst Bin MTPR:** 75dB, **Avg MTPR:** 90dB



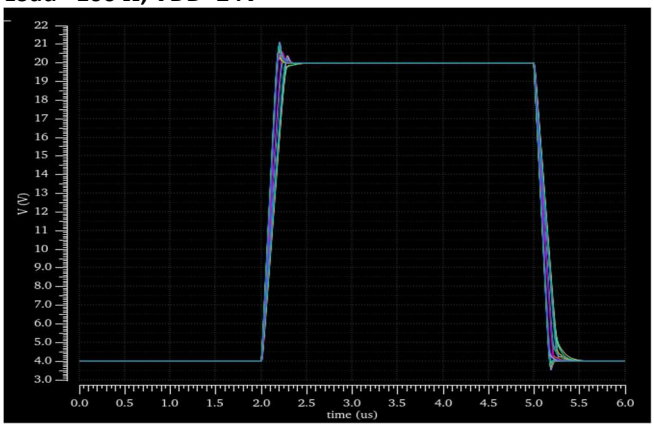
Stability Pulse Tests (low overshoot)

Load = 1 to 1000 Ω, 0 to 2nFd

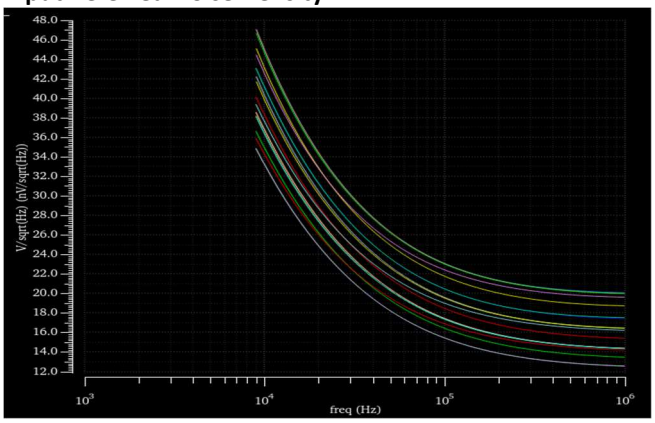


Slew Rate

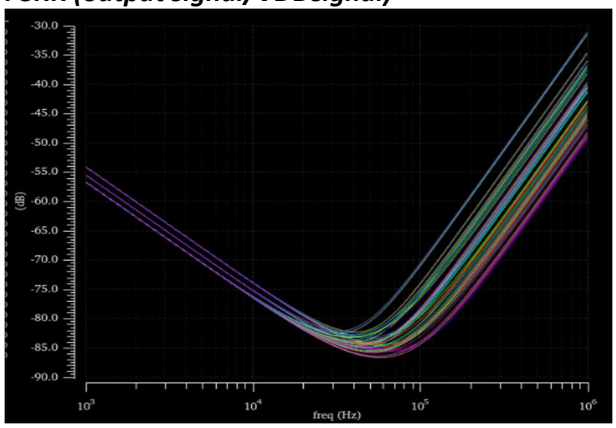
Load =100 Ω, VDD=24V



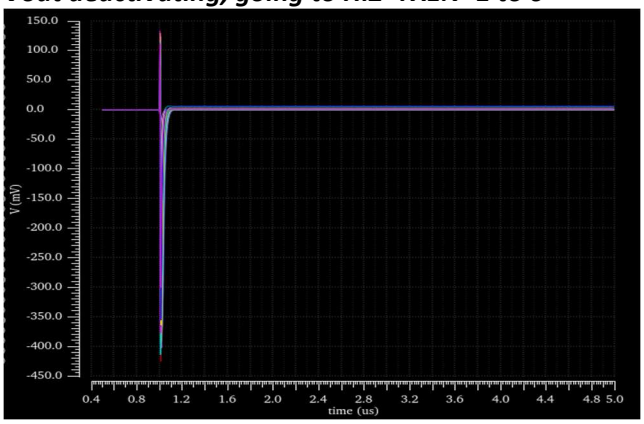
Input Referred Noise Density



PSRR (output signal/VDDsignal)

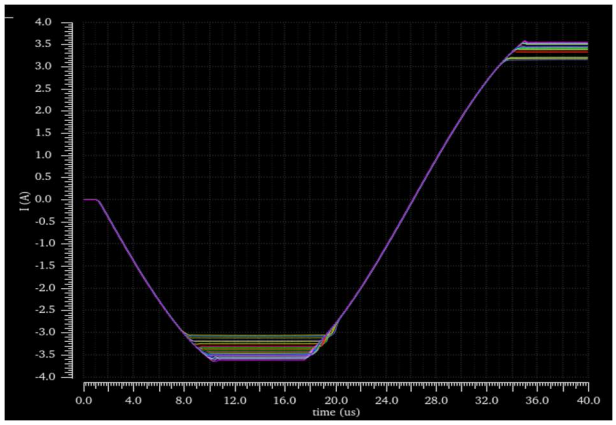


Vout deactivating, going to HiZ TXEN- 1 to 0

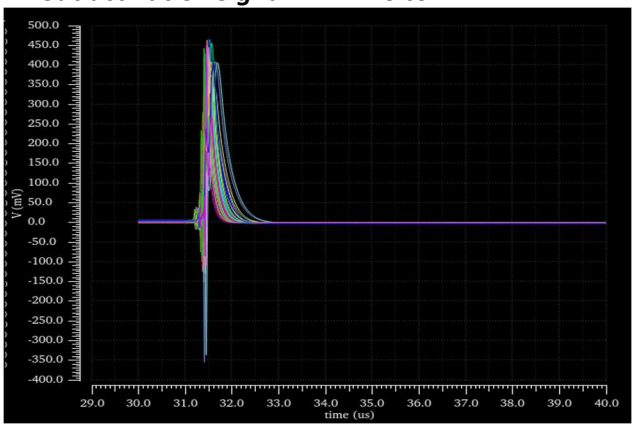


Short Circuit Protection 3.2A

Set to 3.2A current limit VDD=10V
(Full signal is clipped to show the current limit)



Vout activation signal TXEN- 0 to 1



Short Circuit Protection 1.7A setting